

Wire For Liquid Crystal Display And Liquid Crystal
Display Having The Same

**WIRES FOR LIQUID CRYSTAL DISPLAYS,
LIQUID CRYSTAL DISPLAYS HAVING THE SAME, AND
MANUFACTURING METHODS THEREOF**

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BACKGROUND OF THE INVENTION

(1) Field of the invention

The present invention relates to wires for liquid crystal displays (LCDs),
LCDs having the same and manufacturing methods thereof.

10 **(2) Description of the Related Art**

In general, an LCD has a gate wire on a substrate, and the gate wire
includes gate lines, gate pads and gate electrodes which transmits scanning
signals. The gate wire is covered with a gate insulating layer, and a
semiconductor layer is formed on portions of the gate insulating layer opposite
15 the gate electrodes. The LCD also has a data wire on the gate insulating layer,
and the data wire includes data lines, data pads and source electrodes
transmitting image signals and drain electrodes connected to the source
electrodes through the semiconductor layer. A passivation layer having a
contact hole exposing the drain electrode is formed on the data wire, and pixel
20 electrodes which are formed of a transparent conductive material such as ITO
(indium tin oxide) and connected to the drain electrodes through the contact
hole are formed thereon.

To manufacture the liquid crystal display, deposition, photolithography
and etch steps are required for the gate wire, the data wire, the gate insulating

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layer, the passivation layer and the pixel electrodes.

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There are two general methods for depositing a thin film, a chemical vapor deposition (CVD) and a physical deposition. The CVD forms the film by the reaction of vapor phase chemicals that contain the required constituents, while a sputtering which is a kind of physical deposition obtains the film by having energetic particles to strike target to be sputtered physically. The CVD is generally used to form the semiconductor layer and insulating layers such as the gate insulating layer and the passivation layer, and the sputtering is used to form metal layers for the gate wire and the data wire and an ITO layer for the pixel electrodes.

The etch method is divided into two types, wet etch using etchants and dry etch using etching gases.

In particular, when an ITO layer is etched by using an etchant, hydrochloric acid and nitric acid are used. However, it may happen that the etchant penetrates the passivation layer, contacts the data wire and the gate pad, and then erode the data wire and the gate pad. Accordingly, the data wire and the gate pad may be disconnected and/or eroded.

SUMMARY OF THE INVENTION

In view of the above, it is an object of the present invention to provide a data wire highly durable against a chemical reactive etchant.

A wire according to the present invention is made of either molybdenum nitride layer or molybdenum alloy nitride layer.

The manufacturing method of the wires according to the present

invention uses a reactive sputtering method, and the target for the reactive sputtering may be made of a molybdenum alloy including one selected from tungsten, chromium, zirconium and nickel of 0.1 to less than 20 atm %. The reactive gas mixture used for the reactive sputtering may include argon gas and nitrogen gas, and the inflow amount of the nitrogen gas is at least 50% of that of the argon gas.

Because the wires according to the present invention have low etch rate for the ITO etchant including strong acid, the disconnections of the wires are reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a layout view of a thin film transistor (TFT) array panel according to an embodiment of the present invention.

Figs. 2 and 3 show sectional views of the TFT array panel taken along the lines II-II' and III-III' in Fig. 1, respectively.

Figs. 4A-4F are sectional views of the intermediate structures of the TFT array panel shown in Fig. 1 to Fig. 3 manufactured by a manufacturing method according the embodiment of the present invention.

Fig. 5 is a graph illustrating etch rate of a molybdenum-tungsten alloy nitride layer as function of the volume of nitrogen gas as a reactive gas for aluminum and ITO etchants.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of

the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

Fig. 1 shows a layout view of a TFT array panel according to an embodiment of the present invention, and Figs. 2 and 3 show sectional views taken along the lines II-II' and III-III' in Fig. 1, respectively.

The structure of the TFT array panel according to an embodiment of the present invention includes a supplementary wire highly endurable against a chemical reactive etchant to prevent disconnections of signal lines.

A gate wire made of either molybdenum or molybdenum alloy is formed on an insulating substrate 100, and the gate wire has a thickness of 1,000 - 4,000 Å and includes a transverse gate line 200, a gate electrode 210, which is a branch of the gate line 200, and a gate pad 230 which is connected to one end of the gate line 200. A supplementary gate wire 250 having a thickness of 300 - 1,000 Å is formed under the gate wire 200, 210 and 230 and made of

either molybdenum nitride (MoN_x) or molybdenum alloy nitride (Mo-alloy-N_x).

The supplementary gate wire 250 may be located on the gate wire 200, 210 and 230. The molybdenum alloy used in this embodiment comprises one selected from tungsten, chromium, zirconium and nickel of the content of 0.1 to

5 less than 20 atm %.

Sub 24 → A gate insulating layer 300 covers the gate wire 200, 210 and 230, a hydrogenated amorphous silicon (a-si:H) layer 400 and a doped hydrogenated amorphous silicon layer 410 and 420 including N type impurity are sequentially formed on the gate insulating layer 300 opposite the gate electrode 210, and
10 the portions 410 and 420 of the doped amorphous silicon layer are opposite each other with respect the gate electrode 220.

A data line 500 in the longitudinal direction is formed on the gate insulating layer 300, a source electrode 510 which is a branch of the data line 500 is formed on the one portion 410 of the doped amorphous silicon layer, and
15 a drain electrode 520 opposite the source electrode 510 with respect to the gate electrode 210 is formed on the other portion 420 of the doped amorphous silicon layer. Here, the data wire including the data line 500, the source and drain electrodes 510 and 520 is made of either molybdenum or molybdenum alloy.

Sub 25²⁰ → A supplementary data wire 550 made of either molybdenum nitride or molybdenum alloy nitride is formed under the data wire 500, 510 and 530. The molybdenum alloy used in this embodiment comprises one selected from tungsten, chromium, zirconium, and nickel of the content of 0.1 to less than 20

atm %. The supplementary data wire 550 may be located on the data line 500.

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A passivation layer 700 is formed on the data wire 500, 510 and 520 and portions of the amorphous silicon layer 400 which is not covered by the data wire 500, 510 and 520. The passivation layer 700 has a contact hole C1 exposing the drain electrode 520, and another contact hole C2 exposing the gate pad 230 along with the gate insulating layer 300. Here, the description of a data pad connected to the data line 500 is omitted.

Finally, a pixel electrode 700 formed of ITO (indium tin oxide) and connected to the drain electrode 520 through a contact hole C1 is formed on the passivation layer 700. Furthermore, a gate ITO layer 710 connected to the gate pad 230 through the contact hole 720 and improving the contact characteristics is formed on the passivation layer 700.

A manufacturing method of the TFT array panel will now be described specifically with reference to Figs. 4A-4F.

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Figs. 4A-4F show cross sectional views of the intermediate structures of the TFT array panel shown in Fig. 1 to Fig. 3 manufactured by a manufacturing method according to the embodiment of the present invention.

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As shown in Fig. 4A, a nitride layer 251 made of either molybdenum nitride or molybdenum alloy nitride is deposited on a transparent insulating substrate 100 by using reactive sputtering method. The target for the reactive sputtering is made of either molybdenum and molybdenum alloy having one selected from tungsten, chromium, zirconium, and nickel of the content ratio of 0.1 to less than 20 atm %. A reactive gas mixture includes argon gas (Ar) and

nitrogen gas (N_2), and the inflow amount of the nitrogen gas is equal to or more than 0.5 times that of argon gas. Thereafter, a metal layer 201 made of either molybdenum or molybdenum alloy is deposited by sputtering. The metal layer 201 may be deposited before the deposition of the nitride layer 251.

5 As shown in Fig. 4B, the metal layer 201 and the nitride layer 251 are sequentially patterned to form a gate wire including a gate line 200, a gate electrode 210 and a gate pad 230, and a supplementary gate wire 250 by performing a wet etch using an etchant such as aluminum etchant comprising nitric acid, acetic acid, phosphoric acid and dionized water.

Suba¹⁰⁹ As shown in Fig. 4C, a gate insulating layer 300 made from silicon nitride, a hydrogenated amorphous silicon layer and an extrinsic or doped hydrogenated amorphous silicon layer highly doped with N type impurity are sequentially deposited by plasma-enhanced chemical vapor deposition (PECVD hereafter). The amorphous silicon layer and the extrinsic amorphous
15 silicon layer are patterned by photolithography to form an active pattern 401 and 411. A nitride layer 551 made of either molybdenum nitride or molybdenum alloy nitride with the thickness of 300~1,000 Å is deposited by using reactive sputtering method, and a metal layer 501 made of either molybdenum or molybdenum alloy with the thickness of 1,000 - 4,000 Å is
20 deposited. The metal layer 501 may be deposited before the deposition of the nitride layer 551. When the thickness of the nitride layer 551 is less than 300 Å, it is difficult to obtain the uniform thickness, and the thickness of more than 1,000 Å deteriorates the following etch step.

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As shown in Fig. 4D, the metal layer 501 and the nitride layer 551 are sequentially patterned to form a data wire including a data line 500, a source electrode 510, a drain electrode 520 and a data pad (not shown), and a supplementary wire 550 by performing wet-etch using the above-described aluminum etchant. Because the etch rate for the upper metal layer 501 is larger than the etch rate for the low nitride layer 551, the metal layer 501 may be over-etched. Accordingly, it is desirable that the thickness of the nitride layer 551 is less than 1,000 Å to prevent the over-etch of the metal layer 501.

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Thereafter, exposed portions of the extrinsic amorphous silicon layer 411 is removed such that the extrinsic amorphous silicon layer is then divided into two portions 410 and 420, and the central portion of the amorphous silicon layer 400 is exposed.

As shown in Fig. 4E, a passivation layer 600 is deposited and patterned along with the gate insulating layer 300 to form contact holes C1 and C2 exposing the drain electrode 520 and the gate pad 230, respectively

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Finally, an ITO layer is deposited and patterned to form a pixel electrode 700 connected to the drain electrode 520 through the contact hole C1 and a gate ITO layer 710 connected to the gate pad 230 through the contact hole 720 as shown in Fig. 4F. Here, the etchant for the ITO layer comprises hydrochloric acid and nitric acid, which may penetrate along the crack of the passivation layer 600 or along the edges of the ITO wire 700 and 710, and then may reach the data wire 500, 510 and 520, and the gate pad 230.

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However, because the supplementary gate wire 250 and the

supplementary data wire 550 have a low chemical reactivation against the ITO etchant, the gate wire 200, 210 and 230, and the data wire 500, 510 and 520 through the supplementary gate wire 250 and the supplementary data wire 550 are not disconnected.

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Next, the etch rate of a molybdenum-tungsten alloy nitride layer as function of volume of nitrogen gas as a reactive gas for aluminum and ITO etchants is described to confirm the low chemical reactivation of the supplementary gate and data wires 250 and 550 for aluminum and ITO etchants.

10 Fig. 5 is a graph illustrating etch rates of a molybdenum-tungsten alloy nitride layer as function of inflow amount of nitrogen gas as a reactive gas for aluminum and ITO etchants. The horizontal axis indicates the inflow amount of a nitrogen gas in sccm, and the vertical axis indicates etch rates of a molybdenum-tungsten alloy nitride layer in Å/sec for an aluminum etchant and
15 an ITO etchants. In this experiment, the inflow amount 105 sccm of the Ar gas is fixed, and that of nitrogen gas varies from zero to 160 sccm during reactive sputtering. The etch rate of the molybdenum-tungsten alloy nitride layer for the aluminum etchant and the ITO etchant decreases as the inflow amount of nitrogen gas with respect to argon gas increases. Its etch rates for
20 the aluminum etchant and the ITO etchant are respectively 95 Å/sec and 35 Å/sec when inflow amount of argon gas is 105 sccm and that of nitrogen gas is 50 sccm. The etch rate below 35 Å/sec implies that the etched thickness is negligible. In addition, because the mount of the ITO etchant penetrating

along the narrow crack having a width of less than 100 μm of the passivation layer is very small, the etched thickness of below 35 $\text{\AA}/\text{sec}$ is ignorable. In the meantime, the etch rate depends on the ratio of argon gas and nitrogen gas. For example, when the inflow amount of the nitrogen gas is at least 50 % of that of the argon gas, not only the supplementary gate and data wires 250 and 550 is simultaneously etched with the gate wire 200, 210 and 230, and the data wire 500, 510 and 520, but also the supplementary gate and data wires 250 and 550 is rarely etched for the ITO etchant.

In the drawings and specification, there have been disclosed typical preferred embodiments of the present invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.